Application No.: 09/991,142 Docket No.: 21806-00134-US

AMENDMENTS TO THE SPECIFICATION

Please add paragraphs 9 and 10, after paragraph 8 on page 3:

A1

Fig. 26 shows two SiGe HBT bipolar transistors with different subcollectors.

Fig. 27 shows an SiGE varactor and SiGe HBT NPN transistor.

Please replace paragraph 5 on page 4 with the following amended paragraph:

A2

According to one embodiment of the present invention, a semiconductor wafer 10 is provided. The semiconductor wafer 10, is typically silicon, for instance a P- type single crystal silicon substrate, but can be any semiconductor material. Figure 1 shows a P- substrate 12 upon which a photoresist layer 14 is formed. A portion of the resist layer 14 is removed forming a region 16 that exposes the P- substrate [10] 12. A first dopant Arsenic (As) is implanted forming an N+ first subcollector region 18. Figure 2 shows that a second dopant Antimony (Sb) is then implanted into the first subcollector region 18.

Please replace paragraph 3 on page 5 with the following paragraph:

A3

The emitter and extrinsic base is then defined. The next step is to deposit an LTE polysilicon layer 114 (e.g., NPN SiGe EPI base film) followed by the deposition of oxide and silicon layers 116, 118[,120, 122]. This is followed by the step of growing and depositing of the emitter film layers 124, 126. Figure 8 shows the semiconductor wafer 10 after the LTE EPI and base film deposition.

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Please replace paragraph 1 on page 6 with the following paragraph:

A4

The emitter formation is then defined. Figure 11 shows the results of the etching of the emitter opening 132. The emitter window etch is followed by a mask which includes a resist layer 134 as shown in Figure 12. The resist layer 134 is then etched and patterned to provide an emitter window etch region 136 above the emitter opening 132. The next step is the pedestal [2] 112 implant into the emitter opening 132. This step includes an emitter polysilicon layer deposit and the implant. The resist layer 134 is then removed followed by providing an N+ emitter polysilicon layer 138 and the deposit of emitter films 140.

Please replace paragraph 4 on page 6 with the following paragraph:

A5

A salicide block mask is then applied. Figure 15 shows that a mask may then be provided including a resist layer 152. The mask may be etched and patterned to form an NPN spacer and a resistor TiSix block. The patterning of the resist layer 152 is provided over the PCP resistor and N+ resistor region after etching resulting in the formation of an NPN spacer and a resistor space TiSix block and a titanium silicide. Titanium salicide is then formed. Figure 16 shows the semiconductor wafer 10 after the TiSix formation and the removal of the resist layer 152.

Please replace paragraph 2 on page 10 with the following paragraph:

A6

In the present invention, a first bipolar transistor comprising a first subcollector and a second bipolar transistor comprising a second subcollector are formed on a common substrate as exemplified by Figure 26. The second subcollector differs from the first subcollector in impurity type and/or doping concentration, and/or in any other fashion that results in a marked differential in sheet resistance. For example, the first subcollector may comprise an implant does in the $1x10^{16}$ cm^{-2} range and the second subcollector may comprise an implant does in the $1x10^{15}cm^{-2}$

range. Sheet reistance of the $1x10^{16}cm^{-2}$ dose is typically 10 Ω/square whereas $1x10^{15}cm^{-2}$ is near 100 Ω/square. As such, the second subcollector provides a higher resistance and a higher collector base breakdown voltage than the first subcollector. As a practical matter, this resistance differential can be increased by reducing the concentration of the second subcollector still further - e.g. to $1x10^{14}cm^{-2}$ and below. However, the best tradeoff between introducing a sufficient differential in resistance without reducing overall transistor performance appears to bc keeping the first subcollector at a resistivity of about 5-20 Ω/square, and the second at 50-200 Ω/square, respectively.

Please replace paragraph 3 on pages 10-11 with the following paragraph:

The invention may be applied to various integrated circuit structures and substrates. For example, the invention may be applied to epitaxial or non-epitaxial substrate, or to HBTs with Si, SiGe, or SiGeC bases. The base region may comprise a "raised base device". The emitter may be a self-aligned emitter, non-self aligned emitter, or a quasi-self aligned emitter. The higher sheet resistance subcollectors may be applied to devices utilized to provide thermal stability, ESD protection, or a high-power device operations for improved power-to-failure. In particular, ESD protection may be provided by high sheet resistance subcollectors in diodes, varactors, or Schottky elements as exemplified in Figure 27.